## IN THE CLAIMS

## What is claimed is:

1	1.	A circuit that selects between at least two power supplies, comprising:
2		an input receiver coupled to receive an input signal and a drive
3		supply that generates a receiver output signal;
4		a supply comparator having inputs coupled to the at least two
5		power supplies that generates at least one select signal;
6		a select circuit coupled to the at least two power supplies and the
7		drive supply; and
8		a latch coupled to the at least one select signal and to the select
9		circuit.
1	<b>2</b> .	The circuit of claim 1, wherein:
2		the input receiver further includes a driver circuit that receives the
3		input signal and generates an internal input signal, the driver circuit
4	× .	including at least a first driver transistor having a source coupled to the
5		drive supply and a gate coupled to the input signal.
1	<b>3</b> .	The circuit of claim 2, wherein:
2		the driver circuit comprises a complementary-metal-oxide-
3		semiconductor (CMOS) type driver.

1 4. The circuit of claim 2, wherein: 2 the input receiver further includes a first disable device that isolates 3 the driver circuit from at least one power supply in response to an enable signal. 1 5. The circuit of claim 2, wherein: 2 the input receiver further includes a second disable device that 3 couples an output of the driver circuit to the driver supply in response to 4 an enable signal. 1 6. The circuit of claim 1, wherein: 2 the select circuit comprises a multiplexer having inputs coupled to the at least two power supplies that is controlled according to an output of 3 the latch. 4 1 7. The circuit of claim 1, wherein: 2 the latch is enabled in response to a power up signal. 8. A method of controlling a power supply path to an input receiver, comprising the 1 steps of: 2 comparing at least two power supply voltages to one another; 3 setting a latch to indicate one of the at least two power supplies as

a selected supply according to said comparison; and

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6		providing the selected supply to the input receiver according to the
7		setting of the latch.
1	9.	The method of claim 8, wherein:
2		the step of setting the latch occurs substantially during a power-up
3		of an integrated circuit containing the input receiver circuit.
1	10.	The method of claim 8, wherein:
2		the step of setting the latch includes setting the latch to indicate the
3		power supply having the lowest magnitude voltage.
1	11.	The method of claim 8, further including:
2		level shifting an output from the input receiver to generate an output
3		signal that varies between predetermined logic levels regardless of which
4		at least one power supply is selected.
5		•
1	<b>12</b> .	An input receiver circuit, comprising:
2		a comparator circuit that generates a select signal in response to a
3		comparison between at least two power supply voltages;
4		a select circuit that couples one of the at least one power supply
5		voltages to a drive node according to the select signal; and
6		a drive circuit that drives an internal input signal between the
7		potential of the drive node and another predetermined potential in

8 response to an input signal.

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1 13. The input receiver circuit of claim 12, wherein:

the comparator circuit includes a comparator having inputs coupled to the at least two power supplies and an output coupled to a passgate that is enabled in response to a power-up signal having a first value.

**14**. The input receiver circuit of claim 13, wherein:

the comparator circuit can further include a latch having an input coupled to an output of the passgate, and a latch output that provides the select signal, the latch being enabled in response to the power-up signal having a second value.

**15**. The input receiver circuit of claim 12, wherein:

the select circuit comprises a first supply transistor having a sourcedrain path coupled between a first supply voltage and the drive node and a second supply transistor having a source-drain path coupled between a second supply voltage and the drive node.

**16**. The input receiver circuit of claim 12, wherein:

the drive circuit includes a complementary-metal-oxidesemiconductor (CMOS) type driver having an input coupled to receive the input signal and a driver output node that provides the internal input

5	signal.

1	<b>17</b> .	The input receiver circuit of claim 16, wherein:
2		a drive circuit further includes
3		a first enable device coupled between the CMOS type driver
4		and a power supply that provides a low impedance path when an
5		enable signal has a first value, and
6		a second enable device coupled between the drive node and
7		the driver output node that provides a low impedance path when
8		the enable signal has a second value.
1	18.	The input receiver circuit of claim 12, further including:
2		a level shift circuit that receives the internal input signal, the leve
3		shift circuit including
4		a pull-up leg that drives an output node to one of the at least
5		two power supply voltages when the internal input signal has a first
6		value, and
7		a pull-down leg that drives the output node to a different
8		power supply voltage when the internal input signal has a second
9 -		value, the different power supply voltage being different from any of
10		the at least two power supply voltages.